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# Robust Design and Test of Analog/Mixed-Signal Circuits in Deeply Scaled CMOS Technologies

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## 1. Introduction

The proliferation of communication and consumer electronic systems leads to the large demands of high-performance & robust analog/mixed-signal circuits. On the other hand, although deeply scaled CMOS technologies enable greater degrees of semiconductor integration and lower manufacturing cost, the advancements of technologies also introduce several new challenges for VLSI circuit design. The increasing parametric variations and their impacts on circuit performances are becoming key issues which make already complex circuits even more sophisticated in design practice (Nassif, 2001). Give these barriers, designing robust mixed-signal circuits in deeply scaled CMOS technologies become a real challenge for circuit designers.

In this chapter, we propose to solve the problems by first introducing efficient and accurate modeling techniques for large analog/mixed-signal circuit designs with consideration of process variations. Powerful statistical dimension reduction techniques are utilized to make performance modeling of large circuits possible. Then these novel circuit models are used to achieve efficient parametric system performance analysis. In such ways the designers can have the full knowledge of real circuit performances under process variations, which makes it feasible to do robust system topology design and circuit optimization for large mixed-signal systems. The efficient modeling framework is also extended for circuit test purposes, which leads to robust Built-in Self-Test (BIST) circuit design and optimization.

We demonstrate the effectiveness of the proposed ideas with two popular types of mixed-signal circuit examples, Sigma-Delta A/D converters and Phase Locked Loops (PLLs).

For Sigma-Delta ADCs, we present a novel parameterized lookup table (LUT) technique for capturing performances of building blocks in the systems, and use these LUTs to perform topology trade-off analysis and system optimization. Modeling of circuit level nonlinearities, adaptive LUT generation and robust system design are explained in detail with comprehensive experimental results (Yu & Li, 2006 & 2007a).

For PLLs, we discuss building parametric Verilog-A models for charge-pump PLLs and use these models for high-level performance analysis. In order to handle large number of parametric variables, dimension reduction technique is applied to reduce simulation complexities. We apply the obtained system simulation framework to evaluate the efficiencies of parametric failure detecting of different BIST circuits and perform optimization based on the experimental results (Yu & Li, 2007b).

## 2. Robust Sigma-Delta ADCs Design

Sigma-Delta ADCs have been widely used in data conversion applications due to the good resolution. However, oversampling and complex circuit behaviors render the transistor-level analysis of these designs prohibitively time consuming (Norsworthy & et al., 1997). The inefficiency of the standard simulation approach also rules out the possibility of analyzing the impacts of a multitude of environmental and process variations critical in modern VLSI technologies. We propose a lookup table (LUT) based modelling technique to facilitate much more efficient performance analysis of Sigma-Delta ADCs. Various transistor-level circuit nonidealities are systematically characterized at the building block level and the whole system is simulated much more efficiently using these building block models. Our approach can provide up to four orders of magnitude runtime speedup over SPICE-like simulators, hence significantly shortening the CPU time required for evaluating system performances such as SNDR (signal-to-noise-and-distortion-ratio). The proposed modeling technique is further extended to enable scalable performance variation analysis of complex Sigma-Delta ADC designs. Such approach allows us to perform trade-off analysis of various topologies considering not only nominal performances but also their variabilities.

### 2.1 Background of Sigma-Delta ADC design

We briefly discuss the background and difficulties for Sigma-Delta ADC design in this section. Various important circuit nonidealities, which are difficult to model accurately using analytical equations, are also discussed. The two basic components of Sigma-Delta ADCs are modulators and digital filters as shown in Fig. 1. The analog input of the ADC is sampled by a very high frequency clock in the modulator, then the sampled signal is passed through the loop filter to perform noise-shaping. The output of the loop-filter is quantized by an internal A/D converter, producing a bit-stream at the same speed as the sampling clock. The low-pass digital filter in the decimator then removes the out-of-band noise, and the down-sampler converts the high speed bit-stream to high resolution digital codes.

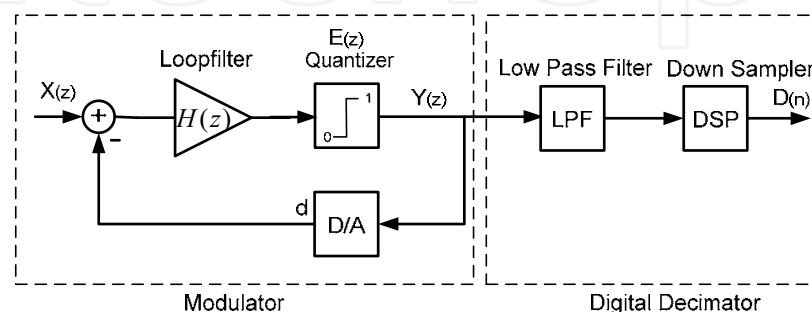


Fig. 1. Block diagram of a Sigma-Delta ADC

The difference between the ideal digital output of the quantizer and the actual analog signal is called quantization noise. The goal of Sigma-Delta technique is to eliminate this unwanted quantization noise as much as possible. By oversampling the input signal, the modulator moves the majority of the quantization noise out of the signal bandwidth. The principle of noise-shaping can be analyzed using transfer functions, which can be obtained using a linear model in the frequency domain. The quantization noise  $E(z)$  is modelled as additive noise to the quantizer, the output of the quantizer  $Y(z)$  can be written as

$$Y(z) = \frac{H(z)}{1 + d \cdot H(z)} \cdot X(z) + \frac{1}{1 + d \cdot H(z)} \cdot E(z) \quad (1)$$

where  $d$  is the feedback gain of the DAC,  $X(z)$  is the input signal,  $H(z)$  is the transfer function of the loop filter. By configuring  $H(z)$  and  $d$ , we can have different noise shaping functions so that the signal-to-noise ratio in the output can be optimized.

Sigma-Delta ADC performances are greatly impacted by various circuit-level nonidealities, such as the finite DC gain, slew of the operational amplifiers, charge injections of the switches, mismatch of the internal quantizers and D/A converters. The effects are difficult to analyze accurately by hand calculation or simple analytical models, neither are their impacts on system performances. There exist several high-level simulators for Sigma-Delta ADC design, like MIDAS (Babii et al., 1997) and SWITCAP (Fang & Suyama, 1992). These techniques are only suitable for architecture-level exploration and determination of building block specifications in the early design phase, but not suitable for the consideration of circuit-level non-idealities. Often the time, transistor-level simulation is the only choice for current performance evaluation, which may take a few weeks for a single transient simulation. Analyzing the impact of process variations is an even greater challenge because a large number of long transient simulations are needed to derive the performance statistics under process variations. In the following sections, we address these issues by adopting the lookup table based models, which can handle the circuit-level details and process variation induced performance statistics accurately and efficiently.

## 2.2 Performance modeling with Lookup table (LUT) technique

The need of efficient simulation techniques capable of including transistor-level details is particularly pressing for assessing the impact of process variations, where the analysis complexity tends to explode in a large parameter space. We start with modelling of switched-capacitor type Sigma-Delta ADCs, which are clocked by some global sampling signals. The major components in the converters are integrators, quantizers and feedback DACs.

Since the switched-capacitor integrators in the discrete-time Sigma-Delta modulators are clocked by the sampling clock as shown in Fig. 2, it is possible to use lookup tables to represent the nonlinear state transfer function of the system (Bishop et al., 1990, Brauns et al., 1990). The output of integrator can be expressed as a function of input signals and their previous states as in (2)

$$y[k+1] = F(y[k], x[k+1], d[k+1]) \quad (2)$$

where  $y[k+1]$  is the current output of the integrator,  $y[k]$  is the integrator output in the previous clock cycle,  $x[k+1]$  and  $d[k+1]$  are the current input signal and the digital feedback

output of the DAC, respectively. This property of Sigma-Delta ADCs makes it possible to predict the new integrator output using the previous state and the new input. The previous state of the integrator, the digital feedback and the new analog input are discretized at a set of discrete voltage levels that are used as the indices to the lookup table models.

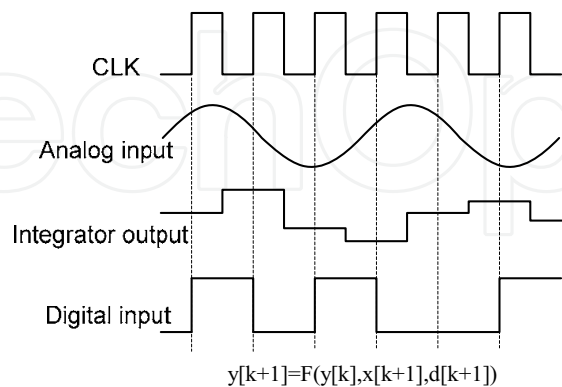


Fig. 2. Integrator behaviours under clocking

As illustrated in equation (2) and Fig. 2, the output of an integrator is a function of the input signals and the initial state of the integrator, which are discretized to generate the lookup table entries. The number of discretization levels depends on the accuracy requirement of the simulation. The internal circuit node voltage swings can be estimated by the system architecture. For low-voltage Sigma-Delta ADC designs, the internal voltages can change from 0 to supply voltage  $V_{dd}$ . To cover the whole range of voltage swing, we discretize the inputs and outputs of the integrators uniformly at  $N$  levels from 0 to  $V_{dd}$ , where  $N$  is in the range of 10. The extraction setup for an integrator with a multi-bit DAC implemented in thermometer code is shown in Fig.3. A large inductor  $L$  together with a voltage source  $V_s$  is used to set the initial value of the integrator output. The input of the integrator is also set by a voltage source  $V_i$ . The digital output of the quantizer controls the amount of charge to be fed back. An  $m$ -bit DAC implemented in thermometer code has  $2^m - 1$  threshold voltages. The digital codes from 0 to  $2^m - 1$  can be represented by counting the number of voltage sources that are connected to the integrator inputs from a set of voltages sources  $V_{d1}, V_{d2}, \dots, V_{d(2^m-1)}$ , the voltages of which are set to be either digital "1" or digital "0".

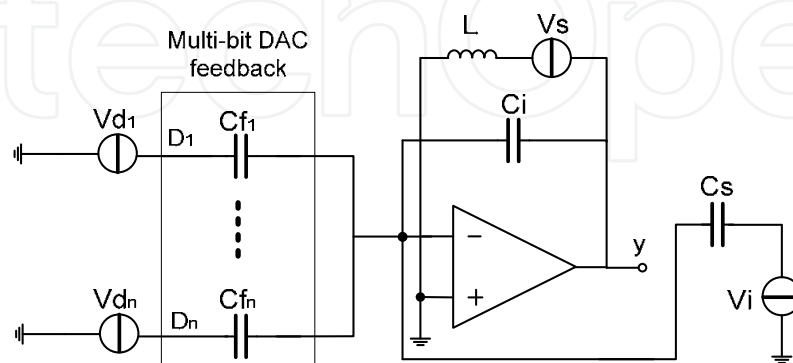


Fig. 3. LUT generation setup for integrators

The nonlinearities of quantizers can be captured using lookup tables as well. The quantizer acts as a comparator, the input threshold voltage varies depending on the direction in which the input voltage changes. To capture the hysteresis effect accurately, we use the transistor-level simulation to find the input threshold voltages at which the digital output switches from 0 to 1 ( $V_{off+}$ ) and from 1 to 0 ( $V_{off-}$ ), respectively. The quantizer is then modeled as

$$d[k+1] = \begin{cases} 1 & (V_{in}[k+1] > V_{off+}) \\ d[k] & (V_{off-} < V_{in}[k+1] < V_{off+}) \\ 0 & (V_{in}[k+1] < V_{off-}) \end{cases} \quad (3)$$

where  $d[k+1]$  is the new output of the quantizer,  $d[k]$  is the output in the previous clock cycle. Multi-bit quantizers can be modeled in a similar way since they are built from several 1-bit quantizers.

Sigma-Delta ADCs with continuous-time modulators can also be modeled using the proposed technique with minor modification. Continuous-time Sigma-Delta ADCs are different from discrete-time counterparts since the integrators are not clocked by the sampling clock, and the input and the output of integrator changes throughout a clock period. In order to make the lookup-based modeling possible, we discretize each clock cycle into  $M$  time intervals with a step size  $dT=T/M$ . If  $dT$  is small enough, then in each small time period the behaviours of continuous-time modulators can be approximated using the presented technique, detailed implementation for continuous-time Sigma-Delta ADCs can be found in (Yu & Li, 2007a).

### 2.3 Parametric LUT based modeling

Process variations in the fabrication stage can cause significant performance shift for analog and mixed-signal circuits. So handling of process variations in the early design stage is critical for robust analog/mixed-signal design. In order to capture the influence of process variations, we extract parameterized LUT models and perform fast statistical simulation to evaluate the performance distributions of complex Sigma-Delta ADCs. Using this efficient modeling technique, we have the ability to find the most suitable system topologies and design parameters for ADC designs.

Since the number of process variables is large, it is not possible to exhaust all the possible performances under process variations. Here we use parameterized LUT-based models to capture the impacts of circuit parametric variations that include both environmental and process variations. In this case, a nonlinear regression model (macromodel) is extracted for each table entry. In general, a macromodel correlating the input variables and their responses can be stated as follows:

given  $n$  sets observed responses  $\{y_1, y_2, \dots, y_n\}$  and  $n$  sets of  $m$  input variables  $[x_1, x_2, \dots, x_m]$ , we can determine a function to relate input  $x$  and response  $y$  as (Low & Director, 1989)



$$\begin{aligned}
 y_1 &= h(x_{11}, x_{12}, \dots, x_{1m}) \\
 y_2 &= h(x_{21}, x_{22}, \dots, x_{2m}) \\
 &\vdots \\
 y_n &= h(x_{n1}, x_{n2}, \dots, x_{nm})
 \end{aligned}
 \tag{4}$$

where

$y_i$	i-th response
$h$	function relating $y$ and $x$
$x_i$	i-th set of process variables
$m$	number of process variables
$n$	number of experimental runs

The task of constructing each macromodel is achieved by applying the response surface modeling (RSM) technique where empirical polynomial regression models relating the inputs and their outputs are extracted by performing nonlinear least square fitting over a chosen set of input and output data (Box et al., 2005). To systematically control the model accuracy and cost, design of experiment (DOE) technique is applied to properly choose a smallest set of data points while satisfying a given modeling regulation. For our circuit modeling task, the input parameters are the parametric circuit variations and the output is an entry in the lookup tables. Then, a nonlinear function such as a quadratic function relating each entry in the tables with the circuit parametric variations can be determined via regression

$$\hat{y} = \hat{\beta}_0 + \sum_{i=1}^m \hat{\beta}_i x_i + \sum_{i=1}^m \sum_{j=1}^m \hat{\beta}_{ij} x_i x_j
 \tag{5}$$

where

$x_i$	i-th process variable set
$Y$	approximated response
$\beta$	estimated model fitting coefficient
$m$	number of process variables

Equation (5) can be rewritten in a more compact matrix form as

$$X \cdot \beta = Y
 \tag{6}$$

The fitting coefficient vector  $\beta$  can be calculated using the least-square fitting of experimental data as

$$\beta = (X^T X)^{-1} X^T Y
 \tag{7}$$

A major problem in solving equations (5 - 7) is the number of experimental data, so a second-order central composite plan consisting of a cube design sub-plan and a star design sub-plan is employed (Box & et al., 2005). The cube design plan is a two-level fractional factorial plan that can be used to estimate first-order effects (e.g.,  $x_i$ ) and interaction effects (e.g.,  $x_i x_j$ ), but it is not possible to estimate pure quadratic terms (e.g.,  $x_i^2$ ). The star design plan is used as a supplementary training set to provide pure quadratic terms in equation (5).

In our implementation, the cube design plan is selected in order to estimate all the first-order and cross-factor second-order coefficient of the input variables.

The ranges of all parametric variations are usually obtained from the process characterization. This information is used to setup the model extraction procedure. In the cube design plan, each factor takes on two values -1 and +1 to represent the minimum and the maximum values of the parametric variation. Each factor in the star plan takes on three levels -a, 0, a, where 0 represents the nominal condition and the level range  $|a| < 1$ . As illustrated in Fig. 4, for each point (i,j) in the lookup table, n simulations runs are conducted using fractional factorial plan to provide the required data to generate the regression model in equation (5). As long as the lookup tables for specified process variation distributions are generated, we can perform fast system-level simulation to evaluate the performances under process variations, and in turn to achieve optimization as to be discussed in the following section.

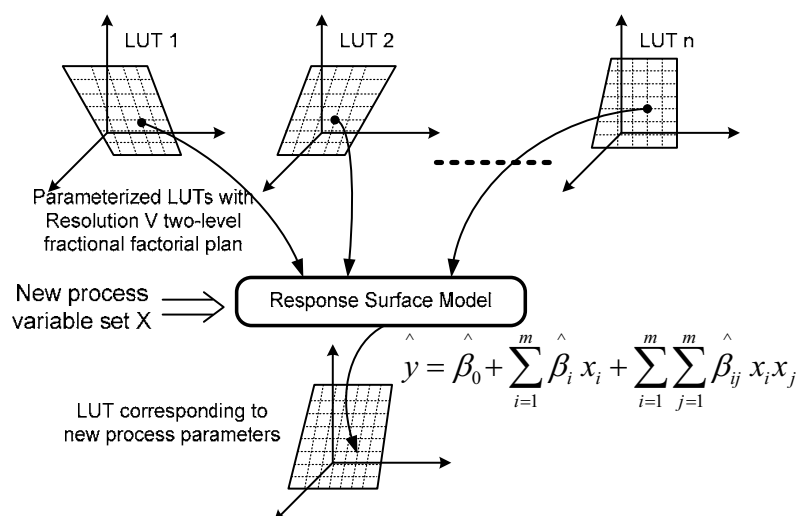


Fig. 4. Response surface modelling of parameterized LUTs

## 2.4 System optimization using parametric LUTs

The application of the proposed modeling techniques are demonstrated with three discrete-time Sigma-Delta ADC designs with different topologies including 2nd-order with 1-bit quantizer (SDM 1), 2nd-order with 2-bit quantizer (SDM 2) and 3rd-order with 1-bit quantizer (SDM 3). All these ADCs are implemented in 130nm CMOS technology with a single 1.5V power supply. The sampling clock and oversampling ratio are chosen to be 1MHz and 128, respectively.

Using our parameterized LUT-based infrastructure, we are able to not only predict the nominal case design performances but also their sensitivities to parametric variations. Hence, our technique provides an efficient way for statistical circuit simulation as well as performance-robustness trade-off analysis. For statistical analysis, a Resolution V  $2^{(8-2)}$  fractional factorial design plan that includes 64 runs for the cube design plan and 17 runs for the star design plan is employed by SDM 1. For SDM 2 and SDM 3, a Resolution VI  $2^{(6-1)}$



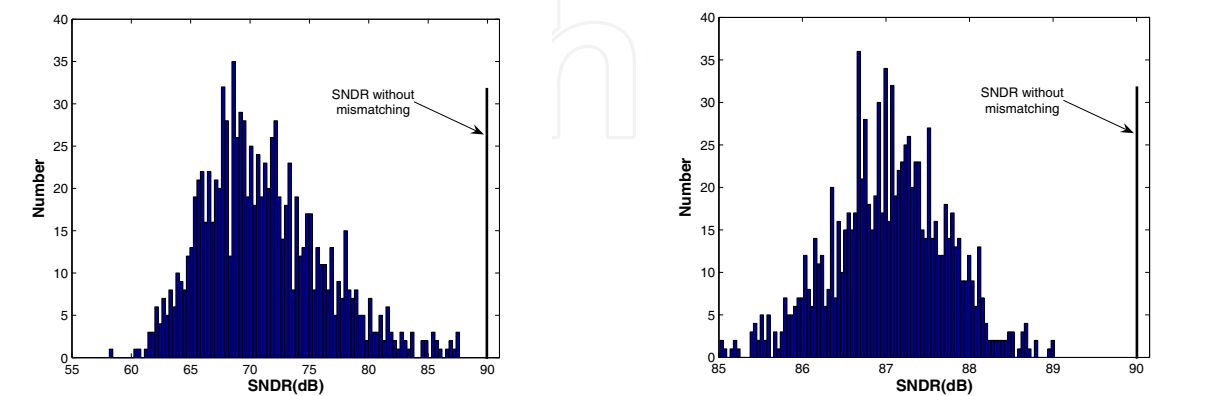
fractional factorial design plan with 45 runs is employed, resulting in 32 runs for the cube design plan and 13 runs for the star design plan.

In Table 1, the proposed LUT-based simulator is compared with the transistor-level simulator (Spectre) in terms of model extraction time, simulation time, and predicted nominal SNDR and THD values. Once the LUT models are extracted, the LUT-based simulator can be efficiently employed to perform statistical performance analysis, which is infeasible for the transistor-level simulator. For the 2nd-order Sigma-Delta ADC with 1-bit quantizer, it only takes 20 minutes to conduct 1,000 LUT-based transient simulations each including 64k clock cycles. For the same analysis, transistor-level simulation with conventional simulators is expected to take 4,500 hours to complete. In terms of accuracy, the SNDRs and THDs predicted by Spectre and the LUT simulator are also presented in Table 1. The error of SNDR of our LUT-based simulator is within 1dB, which demonstrates the accuracy of the proposed technique.

Design	LUT-based simulation					Spectre simulation		
	Sin. gen.	Par. gen.	Runtime	SNDR	THD	Runtime	SNDR	THD
SDM 1	7 min	9.5 hr	2 s	73.8dB	-63.1dB	4.5 hr	74.1dB	-62.6dB
SDM 2	20 min	15 hr	4 s	90.2dB	-77.4dB	9.5 hr	90.0dB	-76.8dB
SDM 3	8 min	11 hr	2 s	83.3dB	-67.5dB	5.5 hr	83.5dB	-66.9dB

Table 1. Runtime and accuracy of the proposed LUT simulation (© [2007] IEEE, from Yu & Li, 2007a)

With the powerful LUT-based simulator, we can perform system evaluation very efficiently so the optimization of system topologies and detailed design become possible. First we use the optimization of 2nd-order Sigma-Delta ADC with multi-bit quantizer as an example by investigating the impacts of DAC capacitance mismatch. The capacitor mismatch level decreases as the capacitance increases, so it is of interest to investigate the trade-offs of system noise performances and area (Pelgrom & et al., 1989). Statistical simulations are performed to analyze the influence of the mismatch of the two internal DACs by sweeping the values of the three charging capacitors in each DAC. The variation of capacitances is modeled using a Gaussian distribution with  $3\sigma = 1\%$ . The distributions of SNDR due to the capacitance mismatch in the two DACs are shown in Fig. 5, respectively.



(a) DAC connected to first-stage (b) DAC connected to second-stage  
Fig. 5. SDNR distributions for DACs connected to different stages in SDM 2 (© [2007] IEEE, from Yu & Li, 2007a)

We can see from the two figures that the mismatch of the DAC connected to the first stage integrator (left figure) has much more influence to the system performance than that of the other DAC (right figure). This can be explained by the fact that the first stage DAC is connected directly to the system input, so the feedback error because of the DAC mismatch will be magnified by the second stage integrator. The result of this analysis indicates that more attention should be paid to the first stage DAC in the design process.

Another optimization example is to evaluate the charging capacitor mismatches in SDM 3. The mismatch of each capacitor is modelled using Gaussian distribution. We evaluate the system performance distributions with variation of capacitances set to  $\sigma = 1\%$  and  $\sigma = 5\%$ , as illustrated in Fig. 6.

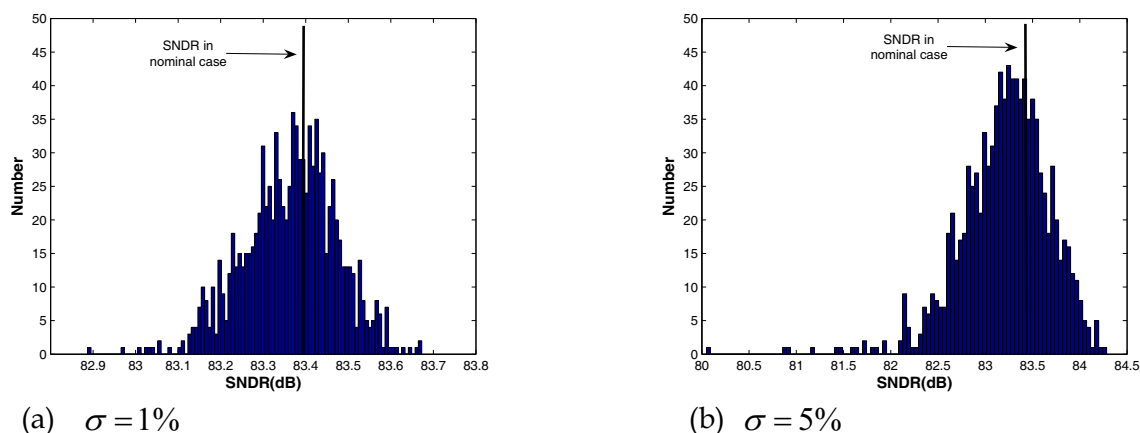


Fig. 6. SNDR distributions for mismatches of charging and sampling capacitors in SDM 3 (© [2007] IEEE, from Yu & Li, 2007a)

We can observe from Fig. 6 that performance distribution deviations increase from 1dB to 4.5dB for capacitor variation  $\sigma = 5\%$ , and the impact of the mismatch of charging and sampling capacitors is not as critical as that of the multi-bit DAC even with  $\sigma = 5\%$ . It is also possible to perform more complete system analysis and optimization using the proposed parametric LUT-based simulation method depending on the target of the design (Yu & Li, 2007a).

### 3. Robust PLL Design

As an essential building block, PLLs are widely used in today's communication and digital systems for purposes such as frequency synthesis, low-jitter clock generation, data recovery and so on. Although the input and output signals of PLLs are in the digital domain, most PLLs implementations consist of both digital and analog components, which make them prone to process variation influences. In this section we propose an efficient parameter-reduction modelling technique to capture process variations and further achieve low-cost system performance evaluation using hierarchical system simulation. The proposed method not only can be used for robust PLL design under process variation, but also paves the road for effective built-in self-test circuit design as to be discussed in the next section.

### 3.1 Background of PLL design

As illustrated in Fig. 7, a typical charge-pump PLL system consists of a frequency detector, a charge pump, a loop filter, a voltage-controlled oscillator (VCO) and a frequency divider. The frequency of the output clock signal  $F_{out}$  is  $N$  times of that of reference clock signal  $F_{ref}$ , where  $N$  can be an integer number or fractional number. The PLL design options include VCO topologies and component sizes, filter characterizations, charge current in the charge pump and so on. The metrics of PLL systems usually include acquisition/lock-in time, output jitter, system power, total area, etc. The goal of PLL design and optimization is to find the best overall system performances by searching in the design variable spaces.

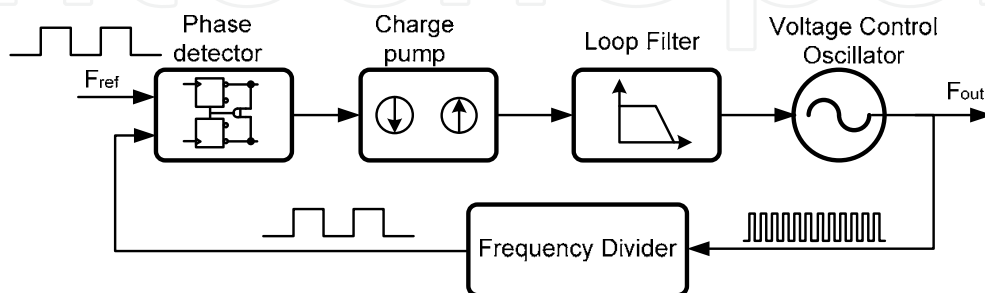


Fig. 7. Block diagram of charge-pump PLL

Due to the mixed-signal nature, the design and optimization of PLL system is quite complex and costly. For example, a long transient simulation (in the order of hours or days) is needed to obtain the lock-in time behavior of PLL, which is one of the most important performance metrics for a PLL. So the brute-force optimization by searching in the design space with transistor-level simulation is infeasible for PLL systems.

The difficulties of system performance analysis can be addressed by adopting a bottom-up modelling and simulation strategy. The performances of analog building blocks can be evaluated and optimized without too much cost. When the behaviours of analog building blocks are extracted, these building blocks can be mapped to Verilog-A models for fast system level evaluation (Zou & et al., 2006). By using this approach we can avoid the scalability issue associated with time consuming transistor-level simulations.

When process variations are considered, the situation becomes more sophisticated. The large number of process variables and the correlations between different building blocks introduce more uncertainties for PLL performance under process variations. In order to utilize the hierarchical simulation method while taking into consideration of statistical performance distributions, we propose an efficient macromodeling method to handle this difficulty. The key aspect of our macromodeling techniques is the extraction of parameterized behavioral models that can truthfully map the device-level variabilities to variabilities at the system level, so that the influence of fabrication stage variations can be propagated to the PLL system performances.

Parameterization can be done for each building block model as follows. First, multiple behavioural model extractions are conducted at multiple parameter corners, possibly following a particular design-of-experiments (DOE) plan (Box & et al., 2005). Then, a

parameterized behavioral model is constructed by performing nonlinear regression over the models extracted at different corners. This detailed parametric modeling step is advantageous since it systematically maps the device-level parametric variations to each of the behavioral models. However, difficulties arise when the number of parametric variations is large, which leads to a prohibitively high parametric model extraction cost. We address this challenge by applying design-specific parameter dimension reduction techniques as described in the following section.

### 3.2 Hierarchical modeling for PLLs

In this section we first describe the nominal behavioral model extraction for each PLL building block, then we discuss how a parameterized model can be constructed in the next section.

The voltage controlled oscillator is the core component of a PLL. The two mainstream types of VCOs are LC-tank oscillators and ring oscillators. In a typical VCO model, the dynamic (response to input change) and static (V-Freq relation) characteristics of the voltage to frequency transfer are modeled separately first and then combined to form the complete model. The static VCO characteristic can be written as  $F_{out}=f(V'_{con})$ , where  $F_{out}$  is the output signal frequency,  $V'_{con}$  is the delayed control voltage, and  $f(.)$  is a nonlinear mapping relating the voltage with the frequency. To generate the analytical model, the mapping function  $f(.)$  can be further represented by an  $n$ -th order polynomial function.

$$F_{out} = a_0 + a_1 V'_{con} + a_2 V'^2_{con} + \dots + a_n V'^n_{con} \quad (8)$$

where  $a_0, a_1, \dots, a_n$  are coefficients of the polynomial. To generate the above polynomial, multiple VCO steady-state simulations are conducted at different control voltage levels and a nonlinear regression is performed using the collected simulation data.

Suppose the control voltage is  $V_{con}$ , the dynamic behavior of the VCO is modeled by adding a delay element that produces a delayed version of the control voltage ( $V'_{con}$ ). The delay element can be expressed using a linear transfer function  $H(s)$  (e.g. a second-order RC network consisting of two R's and two C's).  $H(s)$  can be determined via transistor-level simulation as follows: a step control voltage is applied to the VCO and the time it takes for the VCO to reach the steady-state output frequency, or the step-input delay of the VCO, is recorded.  $H(s)$  is then synthesized that gives the same step-input delay. The dynamic effect is usually notable in LC VCOs due to the high-Q LC tank while in ring oscillators this effect may be neglected.

The charge pump is mainly built with switching current sources. As illustrated in Fig. 8, the control signals of the two switches  $M_1$  and  $M_2$  come from the outputs of the phase and frequency detector. The currents through  $M_1$  and  $M_2$  can be turned on-and-off to provide desired charge-up or charge-down currents. The existing charge pump macromodels are very simplistic. Usually, both the charge-up and charge-down currents are modeled as constant values. A constant mismatch between the two currents may also be considered (Zou & et al., 2006). However, this simple approach is not sufficient to model the behavior of charge pump accurately. In real implementation, the current sources are implemented using transistors so that the actual output currents will vary according to the voltages across these

MOSFETs. Therefore, the dependency of charge-up and charge-down currents on  $V_{con}$  must be considered.

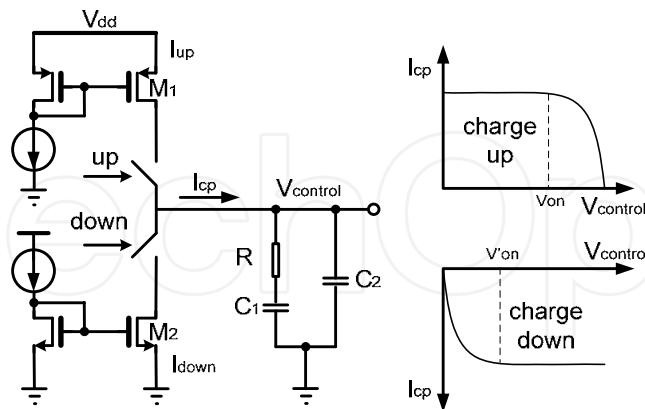


Fig. 8. Modeling of charge pump (© [2007] IEEE, from Yu & Li, 2007b)

In our charge pump model, for each output current, the current vs.  $V_{con}$  characteristics is divided into two regions. When the output voltage  $V_{con}$  is close to the supply voltage, then switch  $M_1$  will be biased in triode region. The charge-up current  $I_{up}$  in the triode region can be written as

$$I_{up} = \mu_p C_{ox} \frac{W}{L} [(V_{gs} - V_{thp})V_{ds} - 0.5V_{ds}^2] \quad (9)$$

$$V_{ds} = V_{dd} - V_{on} - V_{con}$$

where  $V_{dd}$  is the supply voltage,  $V_{on}$  is the on-voltage across the switch,  $V_{gs}$  is the gate-source voltage,  $\mu_p$  is the mobility,  $C_{ox}$  is the oxide capacitance,  $W$  is width and  $L$  is the length of  $M_1$ . We can see from Equation (9) that the charge-up current is dependent on the output voltage  $V_{con}$ . We use a polynomial to explicitly model such voltage dependency

$$I_{up} = b_0 + b_1 V_{con} + b_2 V_{con}^2 + b_3 V_{con}^3 \quad (10)$$

where  $b_i$  are the polynomial coefficients. Similarly, the charge-down current has a strong  $V_{con}$  dependency when  $V_{con}$  is low. This voltage dependency is modeled in a similar fashion. When  $M_1$  and  $M_2$  operate in saturation region, they act as part of the current mirrors. In this case, constant output current values are assumed while the possible mismatches between the two are considered in our Verilog-A models.

The phase detector and the frequency divider are digital circuits so that they are more amenable to behavioral modeling. The two key parameters of the phase detector and the frequency divider are the output signal delay and the transition time, which are easy to extract from transistor-level simulation. The loop filters are usually comprised of passive RC elements, which can be directly modeled in Verilog-A simulation.

### 3.3 Efficient parameter-reduction modeling for PLLs

The key parametric variations for transistors may include variations in mobility, gate oxide, threshold voltage, effective length and so on (Nassif, 2001). The consideration of all possible sources of variations in transistors and interconnects can easily lead to explosion of the



parameter space, rendering the parametric modeling infeasible. Although the widely used principle component analysis (Reinsel & Velu, 1998) can be adopted to perform parameter dimension reduction, its effectiveness may be rather limited since the parameter reduction is achieved by only considering the statistics of controlling parameters while neglecting the important correspondence between these parameters and the circuit performances of interest. As such, the extent to which the parameter reduction can be achieved is not sufficient for our analog macromodeling problems. To address this difficulty, a more powerful design-specific dimension reduction technique, which is based on reduced rank regression (RRR), is developed. This new technique considers the crucial structural information imposed by the design and has been shown to be quite effective for parametric interconnecting modeling problems (Feng & et al., 2006).

Suppose we have a set of  $n$  process variations,  $X$ , and a set of  $N$  performances,  $Y$ . The objective is to identify a smaller set of new variables  $Z$ , based on  $X$ , which are statistically significant to the performances of interest,  $Y$ . Without loss of generality, let us assume  $Y$  nonlinearly depends on  $X$  through a quadratic model

$$Y = f(X) \approx [C_1 \ C_2] \begin{bmatrix} X \\ X \otimes X \end{bmatrix} \quad (11)$$

where  $C_1$  and  $C_2$  are the first and second order coefficients,  $X \otimes X$  represents the quadratic terms of  $X$ . The combination of the linear and quadratic terms of  $X$  are then defined as a new predictor vector  $\tilde{X} = [X^T (X \otimes X)^T]^T$ . Now the quadratic model in equation (11) can be cast

into a linear model as  $Y = A\tilde{X} + \varepsilon$ . To identify the redundancy in  $X$  to facilitate parameter reduction, we seek a reduced rank regression model in the form

$$Y = A_R B_R \tilde{X} + \varepsilon \quad (12)$$

where  $A_R$  and  $B_R$  have a reduced rank of  $R$  ( $R < n$ ), and  $B_R$  has only  $R$  columns. We denote the covariance matrix of  $\tilde{X}$  as  $Cov(X) = \Sigma_{\tilde{X}\tilde{X}}$ , and covariance matrix between  $\tilde{X}$  and  $Y$  as  $Cov(Y, \tilde{X}) = \Sigma_{Y\tilde{X}}$ . It can be shown that an optimal reduced rank model (in the sense of mean square error) is given as (Reinsel & Velu, 1998)

$$A_R = U, B_R = U^T \Sigma_{Y\tilde{X}} \Sigma_{\tilde{X}\tilde{X}}^{-1} \quad (13)$$

where  $U$  contains  $R$  normalized eigenvectors corresponding to the  $R$  largest eigenvalues of the matrix:  $D = \Sigma_{Y\tilde{X}} \Sigma_{\tilde{X}\tilde{X}}^{-1} \Sigma_{\tilde{X}Y}$ . It is important to note that a successful construction of the above reduced rank model indicates that only a smaller set of  $R$  new parameters  $Z = B_R \tilde{X}$  are critical to  $Y$  in a statistical sense, hence facilitating the desired parameter reduction.

It should be noted that the reduced rank regression is only employed as a means for parameter reduction so as to reduce the complexity of the subsequent parameterized macromodeling step. Hence,  $Y$  in the above equations does not have to be the true performances of interest and can be just some circuit responses that are highly correlated to the performances. This flexibility can be exploited to more efficiently collect  $\Sigma_{Y\tilde{X}}$  through Monte-Carlo sampling if  $Y$  are easier to obtain than the true performances in simulation.



The complete parameterized PLL macromodel extraction flow is shown in Fig. 9. Every building block is modeled using Verilog-A for efficient system-level simulation. Each model parameter for building blocks is expressed as a polynomial in the underlying device-level variations, such as

$$P = f(V_{th1}, L_{eff1}, T_{ox1}, \dots, V_{thn}, L_{effn}, T_{oxn}) \quad (14)$$

where  $V_{thi}$ ,  $L_{effi}$ ,  $T_{oxi}$ , etc represent the parameters of  $i$ -th transistor,  $f(.)$  is the nonlinear polynomial function to connect process variations to system performances.  $f(.)$  is very difficult to obtain if the number of parameters is large. Hence, RRR-based parameter reduction is applied, which leads to a set of  $R$  new parameters  $Z$  that are the most important variations for the given circuit performances of interest. If  $R$  is small, then a new parameterized model in terms of  $Z$  can be easily obtained through conventional nonlinear regression for coefficients of equation (11)

$$C = f(Z_1, Z_2, \dots, Z_R) \quad (15)$$

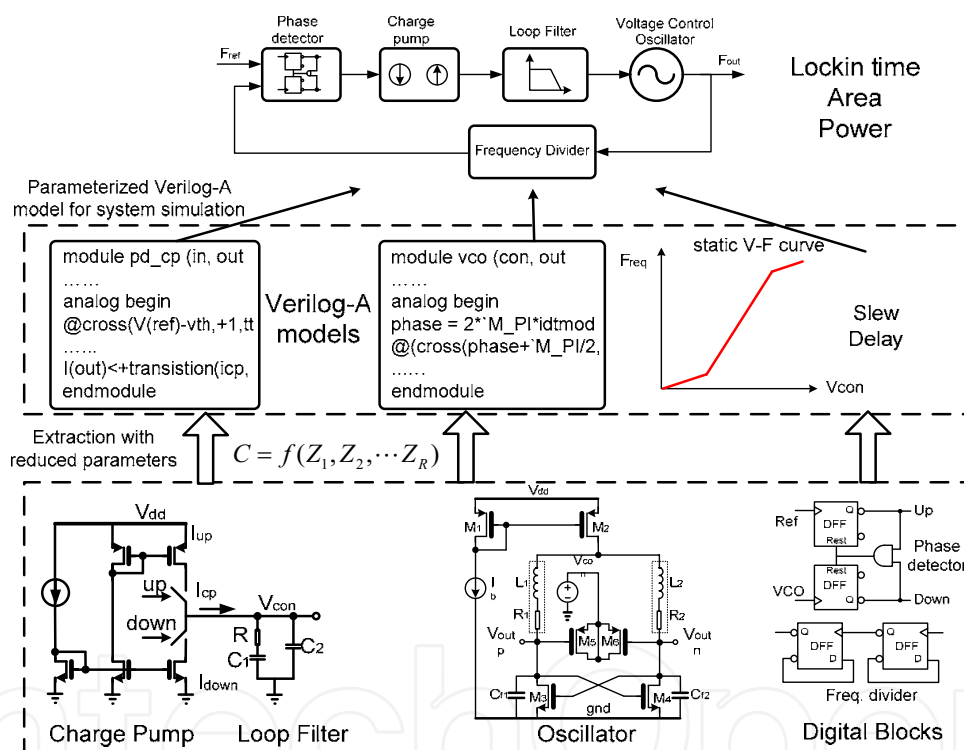


Fig. 9. Flow of PLL macromodeling

In addition to reducing the cost of parameterized macromodeling, parameter dimension reduction will also lead to more efficient statistical simulation of the complete PLL. This is because instead of analyzing the design performance variations over the original high-dimensional parameter space, statistical simulation can now be performed more efficiently in a much lower dimensional space that carries the essential information of the design variability, which is a very good property to achieve PLL system optimization. Detailed optimization method for PLL using the hierarchical macromodels can be found in (Yu & Li, 2008).

With the hierarchical models and parameter reduction technique, we can also perform built-in self-test circuit design and optimization since lengthy transient simulations can be relieved by the proposed method. We will discuss this part in the next section.

#### 4. Built-in Self-test Scheme Design for PLLs

Testing of PLLs is very challenging and of great interest since: a) Usually only simple functional tests such as phase lock test is feasible in production test. However, it may not be sufficient for guaranteeing all the specifications; b) The operation of PLLs is intrinsically complex, e.g. simple frequency domain analysis is not applicable for PLL circuits due to the digitalized input/output signals and the closed-loop dynamics; c) Internal analog signals are difficult to access outside of the chip and system specifications such as jitter, frequency range and lock-time are very complex and costly to measure with digital testers. In this section, we discuss the implementations and optimization of built-in self-test circuits to capture PLL performance failures using the efficient modelling and simulation framework in Section 3.

##### 4.1 BIST circuit design

Built-in self-test (BIST) has emerged as a very promising test methodology for integrated circuits although its application to mixed-signal ICs is more challenging compared to the digital counterparts. Sunter and Roy propose a BIST scheme to measure key analog specifications including jitter, open loop gain, lock range and lock time in PLL systems (Sunter & Roy, 1999), while most of other proposed BIST schemes mainly focus on catastrophic faults. Kim and Soma present an all-digital BIST scheme using charge pump as stimulus to charge VCO up and down to detect catastrophic faults (Kim & Soma, 2001). In (Hsu & et al., 2005) Hsu et al propose a different BIST scheme for catastrophic fault detection in PLLs by introducing the phase errors to the inputs to the phase frequency detector. Other BIST schemes proposed like (Azais & et al., 2003) are also targeted at catastrophic faults.

While detection of catastrophic (hard) faults remains as a key consideration in test, parametric faults caused by the growing process variations in modern nanometer VLSI technologies are receiving significant concerns. In most cases, chips with parametric faults may be still functional but cannot achieve the desired performance specifications, and hence should be screened out. These failing chips are free of catastrophic faults so that specific BIST schemes targeting at parametric failures must be developed.

Given that process variations and resultant parametric failures will continue to rise in sub-100-nm technologies, a design-phase PLL BIST development methodology is strongly desired. Such methodology should facilitate systematic evaluation of parametric variations of complex PLL system specifications and their relations to specific BIST measurements so as to enable optimal BIST scheme development. To this end, however, three major challenges must be addressed: a) Suitable modeling techniques must be developed in order to enable feasible whole system PLL analysis while considering realistic device-level process variations and mismatch; b) Device-level parametric variations and mismatch that contribute to parametric failures form a high-dimensional parameter space and the resulting



Test schemes are described as follows:

a) BIST scheme 1

The first BIST scheme is similar to the one adopted in (Hsu & et al., 2005). In the normal operation mode, the reference input and the output of the frequency divider are applied to the frequency detector to form the closed loop configuration. In the test mode, the output of the frequency divider is disconnected from the input of the frequency detector. The reference input and or its delayed versions are fed through the muxes to the frequency divider forming an open loop configuration. The first delay element has a larger delay value than the second one. To charge up the VCO, the reference input and its delayed version through delay 2 are applied to the frequency detector. To charge down the VCO, the delayed versions of the reference input by both delay 1 and delay 2 are selected. The delay values of the two delay elements determine the phase error introduced at the frequency detector inputs. Hence, they also dictate the coverage of the VCO tuning range in this BIST setup. Under typical design values, delay values in the order of ten's of the reference clock signal period are required, which may cost significant silicon area to implement.

For all these three schemes, the counter read-out signals, which control the start and end points for a single test run, are generated by passing the reference clock signal  $F_{ref}$  through a series of D flip-flops. As such, the contents of the frequency divider within a defined time interval are read out.

b) BIST scheme 2

To solve the silicon overhead problem of scheme 1, we propose the second BIST scheme which employs an inverter to introduce the phase difference. Since this configuration introduces a constant phase delay of  $dT$  at the inputs of frequency divider, the charge pump experiences the following sequence of operation: charge up  $\rightarrow$  stop  $\rightarrow$  charge up  $\rightarrow$  stop until the control voltage of the VCO reaches the fully voltage swing.

c) BIST scheme 3

The third BIST scheme is configured as follows: first the PLL is put in a standard closed-loop configuration and then a standard phase lock test is performed. Once the PLL is locked, the feedback signal frequency is changed from  $F_{out}$  to  $2F_{out}$  by using the mux to select the output of the second last D flip-flop in the divider.

A brief summary of the three BIST schemes: for scheme 1, the area cost is high while the test time is short, for scheme 2, the area cost is low and the test time is also low, for scheme 3, the area cost is low, and the test time is medium. The most important aspect for BIST schemes, however, is the test accuracy. We use the macromodels developed in section 3 to perform test accuracy evaluation and optimization for these BIST scheme candidates.

## 4.2 Test scheme evaluation and optimization

The most straightforward way to evaluate a BIST scheme is to perform Monte-Carlo simulations and examine the ability of the specified BIST measurements to predict the pass/fail status of the design. Since a set of few hundred Monte-Carlo PLL simulations may

take tens of hours to complete, more runtime efficient approaches are needed, especially for the optimization purpose.

The optimization of a given BIST scheme with  $n$  digital outputs is illustrated in the second half of Fig. 11. Since a BIST scheme may be evaluated many times under different setups (e.g., the time interval within which the states of the frequency divider are read out) within the optimization loop, the correlation between the BIST schemes and the PLL performance must be efficiently conducted. This goal is achieved by identifying the critical sources of variations  $Z_v$  as in equation (15).

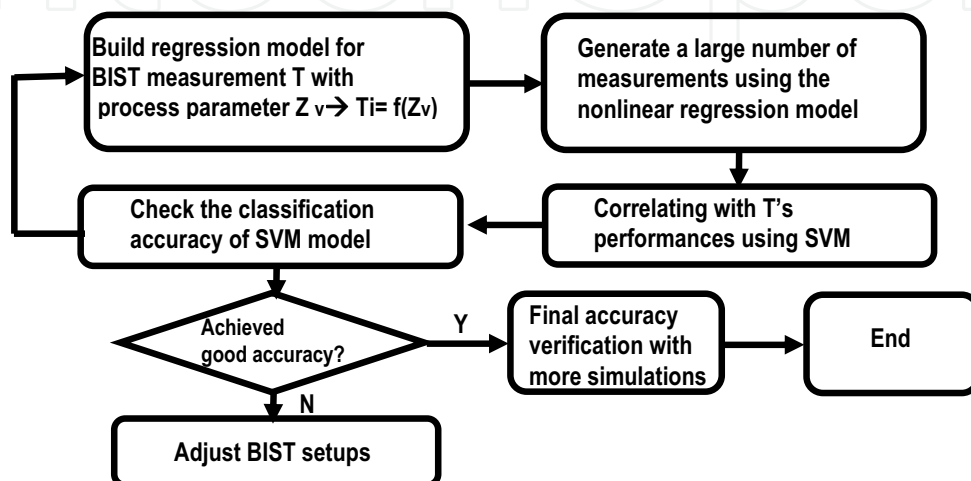


Fig. 11. BIST scheme optimization (© [2007] IEEE, from Yu & Li, 2007b)

Noticing that  $Z_v$  only contains a reduced set of variations, a nonlinear empirical model relating each measurement  $T_i$  of the given BIST scheme and  $Z_v$  can be rather efficiently generated. This is achieved by conducting a few Verilog-A based PLL simulations at different  $Z_v$  samples and performing nonlinear regression:  $T_i = f(Z_v)$ . Note that this step does not incur a high simulation cost since regression models are only built over a low-dimension parameter space represented by  $Z_v$ . Using these easily obtained regression models, a large set of samples for each  $T_i$  can be efficiently generated.

To capture the potential nonlinear correspondence between the design performances and the measurements, Support Vector Machine (SVM) is adopted as an accurate classifier (Vapnik, 1998). Support Vector Machine is a powerful method to build highly nonlinear multivariate regression/classification models. In SVM regression, we consider a set of training data  $\{(x_1, y_1), (x_2, y_2), \dots, (x_n, y_n)\}$ , where  $x_i$  is the input vector and  $y_i$  is the corresponding output. The input  $X$  is mapped into a high dimensional feature space using nonlinear transformation, then a best fitting function is constructed in this feature space as

$$y = f(x) = \omega \cdot \phi(x) + b \quad (16)$$

where  $\phi$  is the nonlinear transformation,  $b$  is the bias term, and  $\omega$  represents the model parameters to be decided. Based on this nonlinear function  $f(\cdot)$ , we can classify the chip as faulty or not with the BIST circuit outputs.

We demonstrate the effectiveness of the proposed method using a PLL design implemented in 90nm CMOS technology. The frequency versus control voltage curve of the VCO is extracted using the model of equation (8). First we simulate the VCO for a few clock cycles and gather the time-domain output response as  $Y$ . Then RRR is applied to get a reduced parameter set  $Z$  to represent the important device-level parameters. A parametric model of the VCO in terms of  $Z$  is then built. To model the statistical characteristics of the VCO accurately, a 6-th order polynomial fitting is used to fit the output frequency vs. control voltage curve.

The Verilog-A models for other building blocks are extracted in a similar fashion. Specifically, the charge pump model is generated using a 3-rd order polynomial in the output voltage for each charge-up/down current. There are a total of 17 Verilog-A model parameters extracted for the complete PLL design.

We evaluate the effectiveness of three BIST schemes. SVM models are generated as in Fig. 11 to predict the pass/fail status of the chips based on the corresponding BIST outputs. 400 Monte-Carlo simulation samples are generated by conducting PLL system simulation using Verilog-A macromodels. These data are used to generate the SVM model. To evaluate the effectiveness of the each scheme more reliably, another 100 Monte-Carlo simulations are carried out and used as the test data for checking the accuracy of the SVM model. The pass/fail predictions achieved through the three SVM models are compared against the simulated chip performances, as shown in Fig. 12. Here, the predictions made through the simulation are labeled as “direct measurement”, and +1 indicates a chip being classified as “fail”, while -1 indicates the opposite.

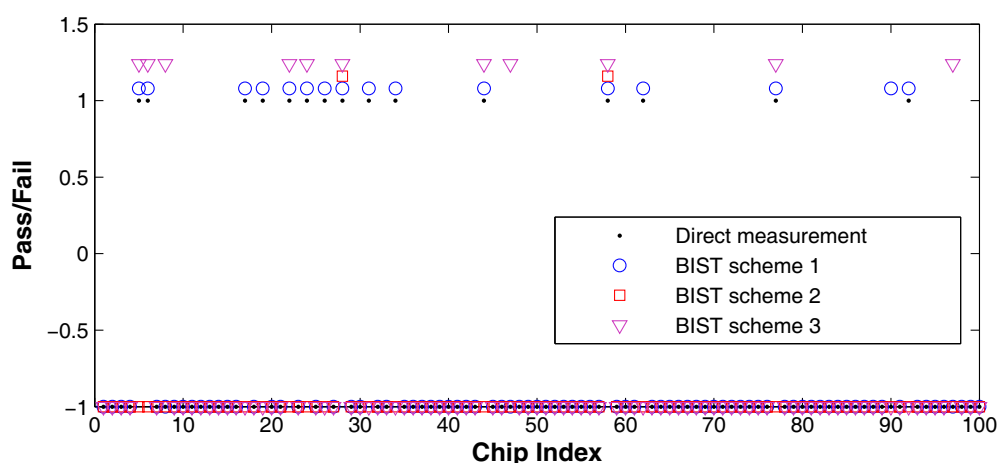


Fig. 12. Pass/fail predictions of three BIST schemes (© [2007] IEEE, from Yu & Li, 2007b)

From Fig. 12 we can see that BIST scheme 1 only has only 1 misclassification. The performance of BIST scheme 2 is verified to be poor as it can only detect two faulty chips which may have largest variations. BIST scheme 3 can detect more failures than scheme 2 but is still not as good as scheme 1.



We further look into the trade-offs between the accuracy and the number of digital outputs for optimization. This is important since fewer test codes will correspond to a shorter test time, if a similar accuracy can be achieved. This trade-off analysis is conducted for every scheme in Fig. 12. It can be observed that for a small number of digital outputs, the accuracy of scheme 2 is actually higher than that of scheme 3. It can be also seen that the accuracy of scheme 3 becomes quickly saturated as the number of outputs increases. Under all the cases, scheme 1 is always the optimal choice.

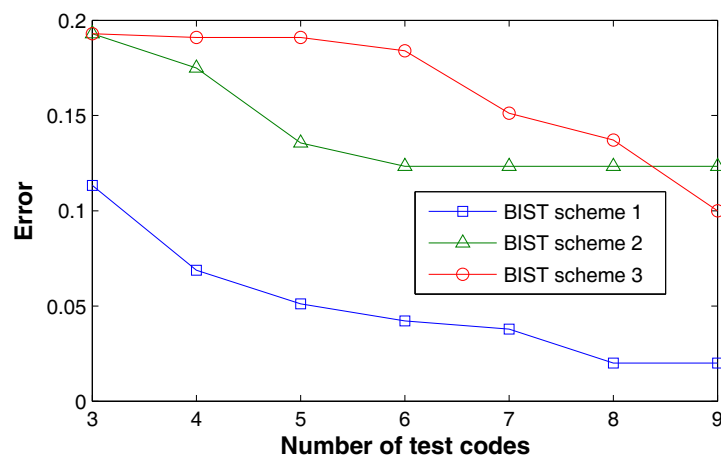


Fig. 13. Accuracy vs. test structures for three BIST schemes (© [2007] IEEE, from Yu & Li, 2007b)

There are other optimizations can be done to improve BIST schemes using the efficient macromodeling technique in Section 3 and Section 4 (Yu & Li, 2007b). It is of great benefit to do such kind of analysis and optimization by taking consideration of statistical system performances in the early design stage so that we can avoid the costly design iterations due to the influence of process and environmental variations.

## 5. Conclusion

In this chapter we have discussed the influences of process variations to analog/mixed-signal circuits in deeply scaled CMOS technologies. The performances of two types of popular mixed-signal systems, i.e. Sigma-Delta ADCs and Phase-locked Loops are evaluated under process variations. Parameterized lookup table technique and reduced-rank regression with hierarchical macromodeling method were proposed to fulfil the optimization of these two systems, respectively. We also extended the obtained fast system performance evaluation framework to compare the efficiencies of parametric failure detecting of different BIST circuits and perform test circuit optimization.

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## **VLSI**

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The process of Integrated Circuits (IC) started its era of VLSI (Very Large Scale Integration) in 1970's when thousands of transistors were integrated into one single chip. Nowadays we are able to integrate more than a billion transistors on a single chip. However, the term "VLSI" is still being used, though there was some effort to coin a new term ULSI (Ultra-Large Scale Integration) for fine distinctions many years ago. VLSI technology has brought tremendous benefits to our everyday life since its occurrence. VLSI circuits are used everywhere, real applications include microprocessors in a personal computer or workstation, chips in a graphic card, digital camera or camcorder, chips in a cell phone or a portable computing device, and embedded processors in an automobile, et al. VLSI covers many phases of design and fabrication of integrated circuits. For a commercial chip design, it involves system definition, VLSI architecture design and optimization, RTL (register transfer language) coding, (pre- and post-synthesis) simulation and verification, synthesis, place and route, timing analyses and timing closure, and multi-step semiconductor device fabrication including wafer processing, die preparation, IC packaging and testing, et al. As the process technology scales down, hundreds or even thousands of millions of transistors are integrated into one single chip. Hence, more and more complicated systems can be integrated into a single chip, the so-called System-on-chip (SoC), which brings to VLSI engineers ever increasingly challenges to master techniques in various phases of VLSI design. For modern SoC design, practical applications are usually speed hungry. For instance, Ethernet standard has evolved from 10Mbps to 10Gbps. Now the specification for 100Mbps Ethernet is on the way. On the other hand, with the popularity of wireless and portable computing devices, low power consumption has become extremely critical. To meet these contradicting requirements, VLSI designers have to perform optimizations at all levels of design. This book is intended to cover a wide range of VLSI design topics. The book can be roughly partitioned into four parts. Part I is mainly focused on algorithmic level and architectural level VLSI design and optimization for image and video signal processing systems. Part II addresses VLSI design optimizations for cryptography and error correction coding. Part III discusses general SoC design techniques as well as other application-specific VLSI design optimizations. The last part will cover generic nano-scale circuit-level design techniques.

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